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INFORMATION DISCLOSURE STATEMENT		Applicants: Shunpei YAMAZAKI et al.							
		Filing Date: February 20, 2002			Group Art Unit: 1762				
U.S. PATENT DOCUMENTS									
Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date (if appropriate)			
<i>Q</i>	2001/0003659	06/14/2001	Aya et al.	<i>RECEIVED JUL 18 2002 TC 1700</i>					
<i>Q</i>	5,643,826	07/01/1997	Ohtani et al.						
<i>Q</i>	5,923,962	07/13/1999	Ohtani et al.						
<i>Q</i>	6,285,042	09/04/2001	Ohtani et al.						
<i>Q</i>	6,335,541	01/01/2002	Ohtani et al.						
FOREIGN PATENT DOCUMENTS									
Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	No		
<i>Q</i>	0 651 431 /	05/03/1995	EP	<i>Full Eng</i>					
<i>Q</i>	07-183540 /	07/21/1995	JP					<i>Eng Abst</i>	
OTHER DOCUMENT (Including Author, Title, Date, Pertinent Pages, Etc.)									
Examiner Initial	<p><i>Q</i> /Kimura et atl., "Device Simulation of Interface Roughness in Laser-Crystallized p-Si TFT's", pp. 263-266, 1999, AM-LCD</p> <p><i>Q</i> /Abe et al., "High-Performance Poly-Crystalline Silicon TFTs Fabricated Using the SPC and ELA Methods", pp. 85-88, July 9-10 1998, AM-LCD</p> <p><i>Q</i> /Specifications and Drawings for Application Serial No. 10/081,767, "Method of Manufacturing a Semiconductor Device" Filing Date: February 25, 2002, Inventors: Shunpei YAMAZAKI et al.</p> <p><i>Q</i> /Specifications and Drawings for Application Serial No. 10/056,054, "Method for Manufacturing a Semiconductor Device"</p>								
Examiner <i>Shunpei YAMAZAKI</i>		Date Considered <i>6/9/03</i>							
<p>*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>									